

AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings includes changes to FIGS. 3, 5 and 6. These sheets, which includes FIGS. 3, 5 and 6, replaces the original sheets including FIGS. 3, 5 and 6.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes



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Formal Drawings for

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6 Sheets / **6** Figures

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US Formals Replacement Sheets

Amended Figures 3, 5, & 6

[illegible]

The diagram illustrates a video signal processing circuit. At the bottom, a horizontal line represents the **VIDEO** input. Four pixel signals, Φ_{PIXEL1} , Φ_{PIXEL2} , Φ_{PIXEL3} , and Φ_{PIXEL4} , are sampled by transistors 202 (controlled by Φ_{RP1} to Φ_{RP4}) and connected to a common node 102. This node is also connected to a feedback path. The feedback path includes a summing junction 108, a feedback capacitor 130, and a feedback resistor 140. The output of the summing junction is V_{OUT} , which is fed back to the input of the first pixel signal through a feedback capacitor 130. The circuit also includes a reference voltage V_{REF} and a feedback capacitor 130. The output of the feedback path is connected to a summing junction 108, which is also connected to a feedback capacitor 130. The output of the summing junction is V_{OUT} , which is fed back to the input of the first pixel signal through a feedback capacitor 130. The circuit also includes a reference voltage V_{REF} and a feedback capacitor 130. The output of the feedback path is connected to a summing junction 108, which is also connected to a feedback capacitor 130. The output of the summing junction is V_{OUT} , which is fed back to the input of the first pixel signal through a feedback capacitor 130.



6/6

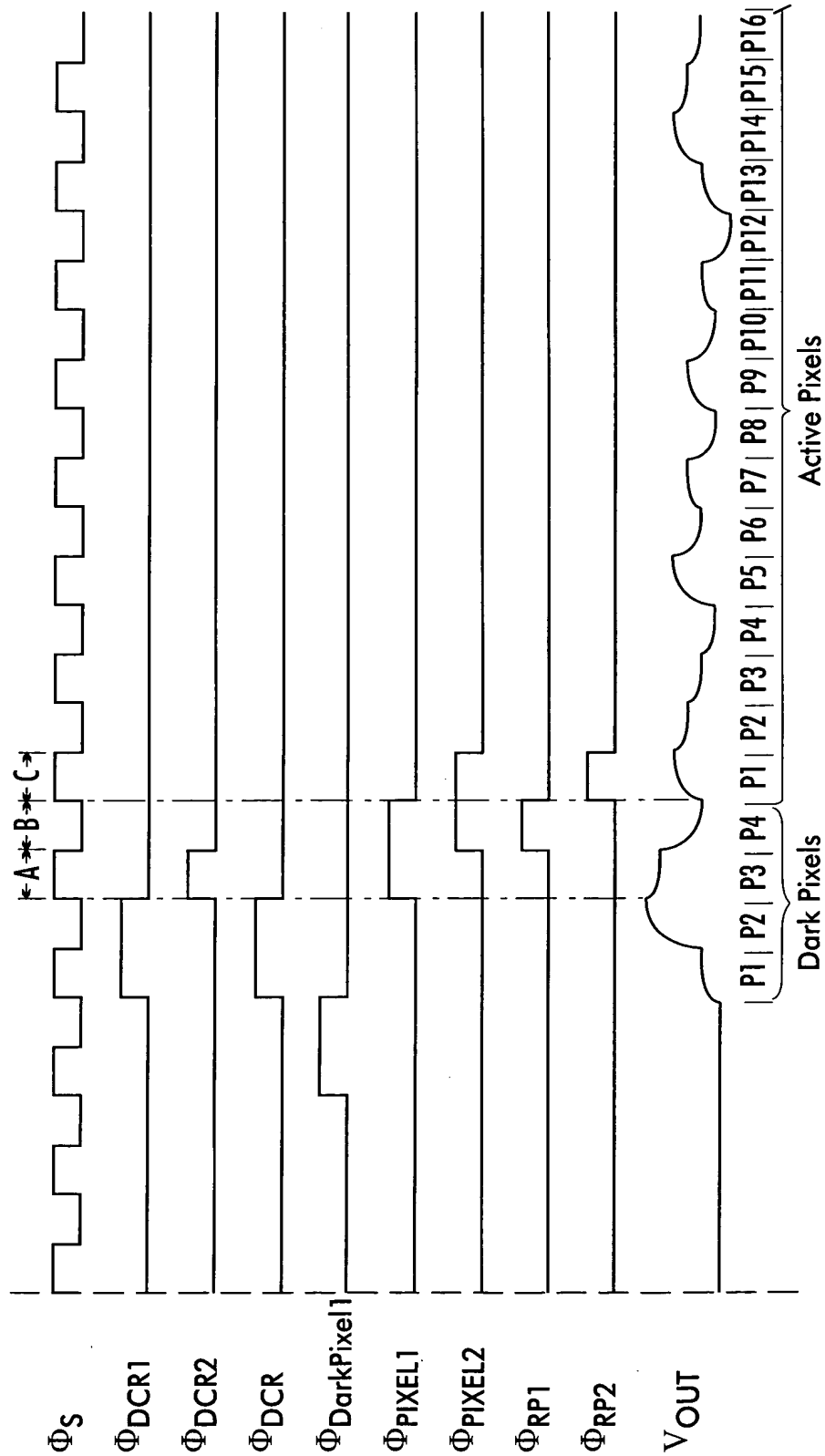


FIG. 6